IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676,p-ISSN: 2320-3331, Volume 11, Issue 5 Ver. III (Sep - Oct 2016), PP 28-33
www.iosrjournals.org

PLL for Grid Synchronization of Single Phase Distributed Generation System

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Abstract: *This paper presents the implementation of an adaptive phase locked loop (EPLL) technique for grid synchronization of single phase distributed generation system(DGS) using a low cost microcontroller. The adaptive PLL consists of a quadrature signal generator(QSG) based on a second order generalized integrator(SOGI) , Parks transform, low pass filter(LF) and frequency phase shift generator(FPG). The QSG-SOGI works as an adaptive notch filter and used for cancellation of harmonic components in the grid voltage. The QSG-SOGI and Parks Transform system is used for enhancing the performance of conventional multiplier based phase detector (PD). The required information about amplitude and phase of grid voltage is extracted from the* v_d *and* v_q *component of PD output. The objective of this paper is to implement the EPLL using a low cost microcontroller for accurate estimation the grid parameters like phase, frequency and voltage amplitude. The experimental results of implementation are discussed in the paper.*

Keywords: *ANF, DGS, ,EPLL, Microcontroller, SOGI*

I. Introduction

The With the increased awareness about the renewable energy sources, policy reforms and net metering, grid connected solar Photovoltaic (PV) are becoming popular and widely used by residential and commercial consumers. In PV system, instead of building large generation farms, it is possible to consider building small energy centers at homes, commercial building and offices that need only a few watts to kilowatts of energy. Such systems in which electrical power is generated and utilized locally are called as "distributed power generation systems" (DGS) [1].The DGS can be grid connected or standalone type. Grid connected system are connected to the utility grid while the stand alone systems operate in islanded fashion. Grid connected systems are more efficient, cost effective and do not require any energy storage.

The grid connected DGS operates in synchronization with utility grid and pumps the active power in the grid. For accurate and rapid power transfer, grid parameters like frequency, phase and magnitude are required. Also the control strategies during the grid fault and islanding detection are based on this information[2].Zero crossing detector (ZCD) is the simplest method of phase and frequency detection. This method detects the zero crossing point of ac voltage and accordingly predicts the phase and frequency. Though simple for implementation, this method is slow and updates the phase and frequency information once or twice in the input signal period[3]. Also it gives very poor performance in the harmonics environment.

For getting the accurate information of synchronization parameters, when the utility grid has harmonics and power quality related issues; use of phase lock loop (PLL) technique has been discussed in the literature[4]-[10]. In PLL, an internal oscillator is used for keeping the track of time and phase of an external periodical signal using a feedback loop.For single phase DGS, Filho et al. [4] has explored three different PLLs arrangement for grid synchronization. Rolim et al. has proposed a robust synchronizing PLL based on the instantaneous real and imaginary power theory (PQ-PLL) to maintain synchronization in presence of sub-harmonics, harmonics, and negative sequence unbalances [5]. PQ-PLL provides the additional information of fundamental positive sequence components along with the phase. The pPLL is distinguished not only for its simple phase error detector but also for its high disturbance rejection. But the pPLL detector has the disadvantage of distorting the system phase error, adding oscillations even under ideal sinusoidal conditions. The other method based on the inverse park transform based PLL (park PLL), is a single-phase version of the synchronous reference frame PLL proposed in which the instantaneous phase angle θ is detected by synchronizing the PLL rotating reference frame to the utility voltage vector[4]. The PI controller sets the direct or quadrature axis reference voltage Vd or Vq to zero, which results in the reference being locked to the utility voltage vector phase angle. Park-PLL provides the information about the utility voltage amplitude and frequency along with the phase[2].

The enhanced PLL (EPLL) is a frequency-adaptive nonlinear synchronization approach which estimates the amplitude, phase, and frequency of the input signal. It has phase detector (PD) mechanism with improved flexibility and provides better information about the amplitude and phase angle of utility voltage.

There are three independent internal parameters for controlling the speed of the amplitude convergence and the rates of phase and frequency convergence[2]-[4].

In this paper an attempt has been made to realize an adaptive filter based PLL for the synchronization of PV based DGS with utility grid polluted with harmonic. The adaptive filter based phase detector is implemented using a Second order Generalized Integrator (SOGI) which has better harmonic rejection characteristics[6]. The algorithm is developed to minimize the computational load on the digital processor so that the PLL can be implemented using a low cost microcontroller as against to the use of high end costly DSP processors. The paper is arranged as follows: Section II discusses about the basics of PLL and use of adaptive filter based PLL applications, Section III discuses the SOGI based quadrature component generation and EPLL, Section IV details about implementation and experimentation results while conclusion is in section V.

II. Basic Phase-Locked Loop

2.1 PLL Structure

The basic structure of a phase-locked loop (PLL) is shown in Fig. 1. It consists of three fundamental blocks as:

Phase detector (PD): This block generates an output signal proportional to the phase difference between the input signal, *v*, and the signal generated by the internal oscillator of the PLL, *v'*. The type of PD decides high-frequency AC components appearing together with the DC phase-angle difference signal[4].

Loop filter (LF*):* This block presents a low-pass filtering characteristic to attenuate the high-frequency AC components from the PD output. Typically, this block is constituted by a first-order low-pass filter or a PI controller.

Voltage-controlled oscillator (VCO): This block generates at its output an AC signal whose frequency is shifted with respect to a given central frequency, ω_c, as a function of the input voltage provided by the LF.

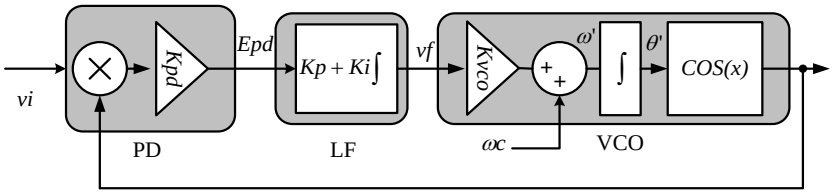


Fig. 1. Block diagram of basic PLL structure

2.2 PLL equations:

In the block diagram of an elementary PLL is shown in Fig.1, the PD is implemented by means of a simple multiplier, the LF is based on a PI controller and the VCO consists of a sinusoidal function supplied by a linear integrator. If the input signal applied to this system and the signal generated by the VCO is given by equations (1) and (2),

$v = V sin\,\theta = V\,sin(\omega t + \emptyset)$ (1)

$v' = cos\,\theta = \cos(\omega' t + \emptyset')$ (2)

the phase error signal from the multiplier PD output can be written as

$$e_{pd} = \frac{Vk_{pd}}{2}[\sin((\omega - \omega')t + (\emptyset - \emptyset')) + \sin((\omega - \omega')t + (\emptyset + \emptyset'))] \quad (3)$$

As the high-frequency components of the PD error signal will be filtered out by the LF, only the low-frequency term will appear on output given by equation

$$e'_{pd} = \frac{Vk_{pd}}{2}[\sin((\omega - \omega')t + (\emptyset - \emptyset'))] \quad (4)$$

With properly tuned VCO $\omega \approx \omega'$, the DC term of the phase error signal is given by

$$e'_{pd} = \frac{Vk_{pd}}{2}[\sin(\emptyset - \emptyset')] \quad (5)$$

It can be observed in (5) that the multiplier PD produces nonlinear phase detection because of the sinusoidal function.

However, when the phase error is very small, i.e. when

$\emptyset \approx \emptyset'$, the output of the multiplier PD can be linearized in the vicinity of such an operating point since $\sin(\Phi - \Phi') \approx \sin(\theta - \theta') \approx (\theta - \theta')$. Therefore, once the PLL is locked, the relevant term of the phase error signal is given by

$$e'_{pd} = \frac{Vk_{pd}}{2}[(\theta - \theta')] \quad (6)$$

This equation can be used to implement a small signal linearised model of the multiplier PD. In the locked state, this model represents a zero-order block whose gain depends on the input signal amplitude.

2.3 PLL Linearised Small Signal Model

The equations (1-6) in the time domain can be very easily translated to the complex frequency domain by using the Laplace transform. If it is considered that *kpd* = *kvco* = 1, the output of phase detector, loop filter and VCO blocks can be given by (7),(8) and (9) respectively,

$$e_{pd} = \frac{V}{2}(\emptyset(s) - \emptyset'(s)) \qquad (7)$$

$$V_{LF}(S) = k_p\left(1 + \frac{1}{T_i(s)}\right)e_{pd} \qquad (8)$$

$$\theta'(S) = \frac{1}{S}V_{LF}(S) \qquad (9)$$

Thus the closed loop error transfer function of block diagram in fig.1 can be given as

$$E_\theta(S) = \frac{S^2}{S^2 + K_p S + \frac{K_p}{T_i}} \qquad (10)$$

The open loop transfer function of PLL reveals that the PLL is a type 2 system, with two poles at the origin, indicating that PLL system can track constant slope ramp in the input phase-angle without any steady-state error. Also the PLL has low-pass filtering characteristic in the detection of the input phase-angle, which attenuates the detection error caused by noise and high-order harmonics in the input signal. The second-order transfer functions can be written in a normalized way as follows:

$$H_\theta(S) = \frac{2\xi\omega_n S + \omega_n^2}{S^2 + 2\xi\omega_n S + \omega_n^2} \;\&\; G_\theta(S) = \frac{S^2}{S^2 + 2\xi\omega_n S + \omega_n^2} \quad (11)$$

Where $\omega_n = \sqrt{\frac{K_p}{T_i}}$ and $\xi = \frac{\sqrt{K_p T_i}}{2}$

Above expressions are useful for obtaining the rough estimate of tuning parameters of the PI controller.

2.4 Structure of EPLL

In three phase system, Clarkes transform is used for conversion of three phase quantities in to two synchronously rotating quadrature components. SOGI based QSG is used in single phase system for introducing a pseudo quadrature component and the vector approach can be used. The orthogonal and stationary reference frame defined by the *αβ* axes, gives rise to the virtual input vector ***v***. Then the output signals of the Park transformation are represented by the projections of the voltage vector ***v*** on an orthogonal and rotating reference frame defined by the *dq* axes and given by

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos(\theta') & \sin(\theta') \\ -\sin(\theta') & \cos(\theta') \end{bmatrix}\begin{bmatrix} v_\alpha \\ v_\alpha \end{bmatrix} \qquad (12)$$

For a well tuned PD, $\omega \approx \omega' and\ \theta \approx \theta'$ and (12) equation can be written as

$$v_{dq} = \begin{bmatrix} v_d \\ v_q \end{bmatrix} = V\begin{bmatrix} \sin(\theta - \theta') \\ -\cos(\theta - \theta') \end{bmatrix} \qquad (13)$$

The input voltage $v_\alpha = V\ sin(\theta)$, can be understood as the projection of the input voltage on the stationary α axis. The angular position of the *dq* rotating reference frame, θ, is given by the PLL. When the PLL is well tuned to the input frequency ($\omega \approx \omega'$), the virtual input vector and the *dq* reference frame have the same angular speed. Under perfect lock conditions, one of the axes of the *dq* reference frame will overlap the virtual input vector v. The PI regulator of the LF will set the angular position of the *dq* reference frame to make *vd = 0* in the steady state, which means that the input vector *v* will rotate orthogonally to the *d* axis of the rotating reference frame. In other case, if the PI regulator is connected to the *vq* output of the PD, as shown in Fig.4, the virtual input vector *v* will rotate, overlapping the *d* axis of the *dq* reference frame in the steady state. In such a case, the v_d signal will provide the amplitude of the input voltage vector and the phase-angle detected by the PLL will be in-phase with the virtual input vector *v*, which means that the detected phase-angle will be 90◦ lagged with respect to the one of the sinusoidal input voltage, i.e. $\theta' = \theta - \pi/2$[2].

Thus the digital implementation EPLL structure shown in fig.2, grid phase, amplitude and frequency can be accurately estimated.

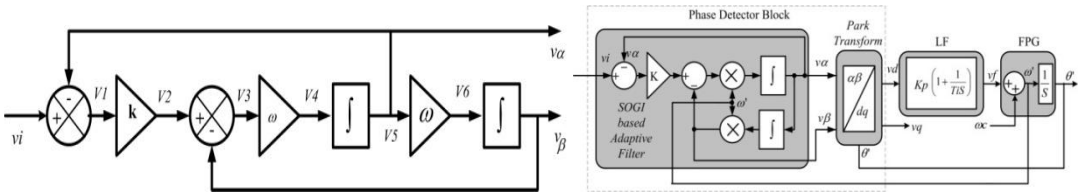


Fig.2(a) Basic SOGI structure. (b)SOGI-QSG & Parks Transform based Phase detector

III. Implementation

3.1 Hardware Description:

The the hardware setup for grid synchronization consists of a potential transformer (PT), signal conditioning circuit and microcontroller. The low voltage output of the PT is further conditioned using a signal conditioning circuit and given to the ADC pin of the microcontroller. LM336 based precision reference circuit is used to generation of stable reference voltage (Vref) of 2.56 for accurate digital conversion.

3.2 Signal Conditioning Circuit

The potential transformer is rated for 300V/12V giving a bipolar voltage signal in the range of ±12Volt rms. To make the signal compatible with microcontroller ADC pin, it is suitably attenuated. The signal peak to peak excursion is restricted between ±1.28 V using a resistance divided arrangement. Then the signal is given to initial buffer stage of signal conditioning circuit. The level shifter stage adds a dc offset voltage of 1.28V, making the output to be in the 0-2.56V range. The precision rectifier in the next stage prevents any excursion of negative voltage. A 3.3 volt zener diode connected at the output stage prevents any overvoltage.

A stable voltage reference of 2.56 V is obtained using LM336. LM336 is operated in temperature compensated mode to minimize the effect of temperature drift on it's output. LM 324 based circuit is used to get precise dc offset voltage of 1.28V.

3.2 Microcontroller description

To validate the EPLL, a standalone system has been realized using Atmel 8/16 bit microcontroller ATXMEGA64A3U. The microcontroller has maximum operating frequency of 32Mhz, 12 bit two channel ADC,12 bit DAC, 8 channel event system, 4 channel DMA and 32 bit timers. Grid voltage is used as input to the PLL. The input signal is sampled at sampling frequency of 10 kHz and to maintain the uniformity in the sampling, ADC operation is triggered using a 100μsec timer. The digital equivalent of the input signal is stored in the RAM using DMA. Event system is used for the sampling process to minimize the processing time of the controller. Advantage of event based programming over the interrupt based programming is the reduced or no intervention of processor for performing the scheduled activities. This saves considerable time required for attending the ISR, otherwise.

3.4 Firmware Description: The various routines used in the firmware development are as follows:

SOGI implementation

This routine is the digital implementation of block diagram shown in fig.2(a). It has two integrations along with multiplication and feedback. The integration constants decide the bandwidth and harmonic filtering. Similarly, the *Ki* decides the dynamics of the response and settling time. Based on the sampling frequency and harmonics filtering considerations, the proportional and integral constants are selected as 5 and 0.1 respectively for the implementation. SOGI routine generates the quadrature component of the input signal and also provides the harmonics filtering.

Parks Transform routine

This subroutine transfers the stationary reference frame quadrature components (v_α and v_β) to the synchronous reference components(*vd* and *vq*). Look up table is used for generating the sine and cosine values corresponding to θ and Parks transform is implemented using the equ.15. Frequency and phase are the offsets used for quick selection of sine and cosine values. The direct component (*vd*)obtained gives the magnitude of the input voltage while quadrature component*(vq)* is used for the calculation of phase and frequency.

LPF and VCO

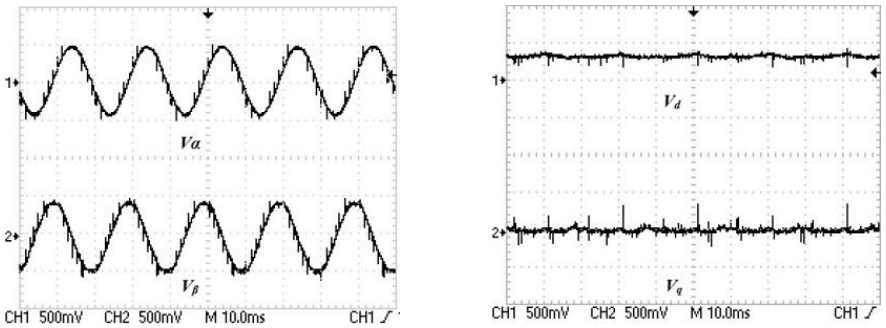
To extract the phase information, the v_q component is digitally processed using PI block with reference to *wc* to get the angular frequency. The *w* is integrated to get the phase of the input signal.

All the routines are developed using assembly language programming. The total cycles and execution time required by different routines is given in Table 1. The on chip 12 bit DAC of microcontroller is used for real time monitoring of all the calculated quantities.

IV. Experimentation And Results

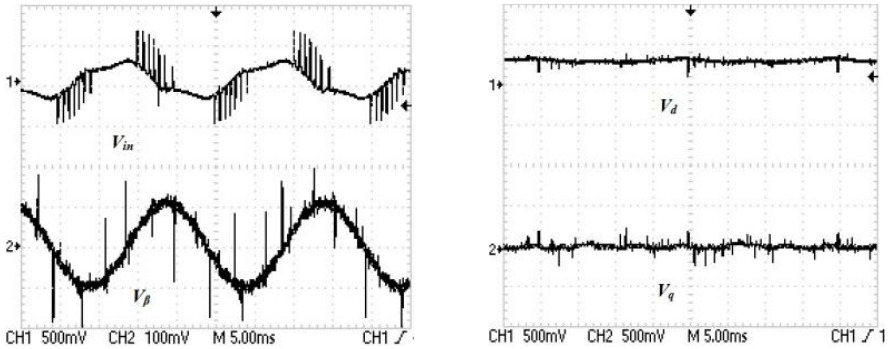
Fig.3(a) shows the waveforms for v_α and v_β i.e. the output of SOGI-QSG block under a steady state conditions where v_α is in phase with the grid voltage while the v_β lags by $\pi/2$ to the grid voltage. The waveforms for v_d and v_q under a condition $\omega=\omega'$ i.e. loop is perfectly locked are shown in fig 3(b). The v_d is proportional to the amplitude of input signal.

To validate the performance of EPLL under harmonic conditions, a distorted wave form is applied to the SOGI-QSG. Fig.4(a) shows the input and output of QSG-SOGI. It can be observed that, though the input is highly distorted, the components v_α and v_β generated by SOGI are sinusoidal. v_α is in phase with the fundamental component of input and v_β is in quadrature. This shows that the SOGI- QSG exhibits excellent noise cancellation characteristics. As the output of SOGI-QSG is used by for the extraction of Phase and frequency information, it remains unaffected due to noise and harmonics. Fig 5(a) and (b) the linear variation of phase of the input signal for sinusoidal and distorted input conditions.



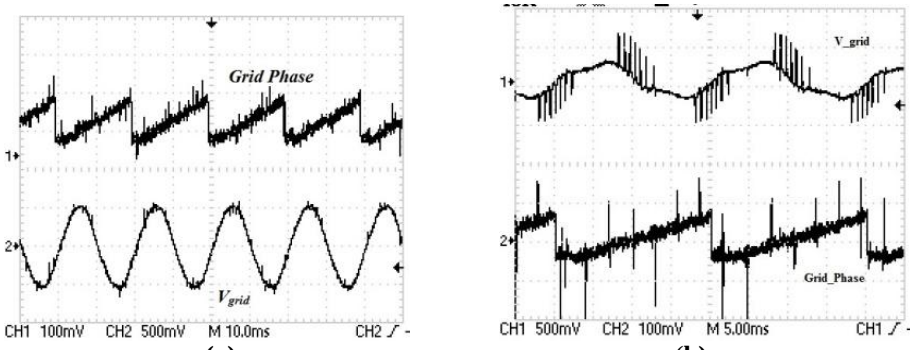
(a) **(b)**

Fig.3. Output of ANF phase detector with sinusoidal input (a) quadrature components (b) Synchronous reference frame components.



(a) **(b)**

Fig. 4. Output of ANF phase detector with distorted input (a) quadrature components (b) Synchronous reference frame components.



(a) **(b)**

Fig. 5. Phase detection (a) with sinusoidal input, (b) distorted input.

Table I CPU Cycle & Execution Time

Process	Cycle	Execution time @ 32Mhz(µsec)
SOGI	143	4.47
PARK Transform	145	4.53
LPF	183	5.71
FPG	102	3.18
Total	573	17.89

V. Conclusion

A detailed analysis of adaptive PLL using SOGI-QSG is discussed in this paper. The SOGI-QSG and Parks transform based phase detector is used to replace the conventional multiplier based PD in PLL. This improves the noise immunity of PLL and can be used under harmonics environment. Also this PLL provides the accurate information about the input signal amplitude and frequency which is essential for designing the power control strategies in grid connected DGS. Implementation using low cost microcontroller makes the solution an affordable option for large scale use of grid connected DGS.

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